Claims

What is claimed is:

1. A memory cell for use in a magnetic random access memory (MRAM) circuit, the memory cell comprising:

a first transistor formed in a semiconductor layer, the first transistor comprising first and second source/drain regions and a gate;

at least a second transistor formed in the semiconductor layer, the second transistor comprising first and second source/drain regions and a gate;

a first insulating layer formed on at least a portion of the first and second transistors;

a first magnetic storage element formed on the first insulating layer, the first magnetic storage element being electrically connected to the first transistor;

at least a second insulating layer formed on at least a portion of the first magnetic storage element; and

at least a second magnetic storage element formed on the second insulating layer, the second magnetic storage element being electrically connected to the second transistor.

2. The memory cell of claim 1, wherein:

the first magnetic storage element comprises first and second terminals, the first terminal of the first magnetic storage element being electrically connected to a first bit line and the second terminal of the first magnetic storage element being electrically connected to the first source/drain region of the first transistor;

the second magnetic storage element comprises first and second terminals, the first terminal of the second magnetic storage element being electrically connected to a second bit line and the second terminal of the second magnetic storage element being electrically connected to the first source/drain region of the second transistor; and

the second source/drain regions of the first and second transistors are electrically connected together.

3. The memory cell of claim 1, wherein at least one of the first and second magnetic storage elements comprises a magnetic tunnel junction (MTJ) device.

4. The memory cell of claim 1, wherein at least one of the first and second insulating layers comprises an oxide.

5. The memory cell of claim 1, wherein the first and second magnetic storage elements are substantially aligned along a vertical dimension relative to one another.

6. The memory cell of claim 1, wherein the first and second magnetic storage elements are substantially non-overlapping relative to one another.

7. The memory cell of claim 1, further comprising:

a first conductive via electrically connecting the first magnetic storage element to the first transistor; and

at least a second conductive via electrically connecting the second magnetic storage element to the second transistor.

8. The memory cell of claim 7, further comprising a first interconnect and at least a second interconnect, a first end of the first interconnect being connected to the first magnetic storage element and a second end of the first interconnect being connected to the first conductive via, a first end of the second interconnect being connected to the second magnetic storage element and a second end of the second interconnect being connected to the second conductive via.

9. The memory cell of claim 7, wherein at least one of the first and second conductive vias comprises a metal.

10. The memory cell of claim 1, wherein the memory cell is configured such that a first write word line is formed on the first insulating layer and in close relative proximity to the

first magnetic storage element, and at least a second write word line is formed on the second insulating layer and in close relative proximity to the second magnetic storage element.

11. The memory cell of claim 1, wherein the memory cell is configured such that first and second read word lines are coupled to the gates of the first and second transistors, respectively, for selectively accessing the first and second magnetic storage elements, respectively.

12. The memory cell of claim 1, wherein the memory cell is configured such that a bit line coupled to the memory cell is shared between the first and second magnetic storage elements associated with the memory cell.

13. The memory cell of claim 1, wherein the memory cell is configured such that a first write word line coupled to the memory cell is shared between the first and second magnetic storage elements associated with the memory cell.

14. A magnetic random access memory (MRAM) array, comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a first transistor formed in a semiconductor layer, the first transistor comprising first and second source/drain regions and a gate;

at least a second transistor formed in the semiconductor layer, the second transistor comprising first and second source/drain regions and a gate;

a first insulating layer formed on at least a portion of the first and second transistors;

a first magnetic storage element formed on at least a portion of the first insulating layer, the first magnetic storage element being electrically connected to the first transistor;

at least a second insulating layer formed on at least a portion of the first magnetic storage element; and

at least a second magnetic storage element formed on at least a portion of the second insulating layer, the second magnetic storage element being electrically connected to the second transistor; and

a plurality of bit lines and word lines operatively coupled to the memory cells for selectively reading and writing one or more memory cells in the MRAM array.

15. The MRAM array of claim 14, wherein:

the first magnetic storage element in the at least one memory cell comprises first and second terminals, the first terminal of the first magnetic storage element being electrically connected to a first bit line and the second terminal of the first magnetic storage element being electrically connected to the first source/drain region of the first transistor;

the second magnetic storage element in the at least one memory cell comprises first and second terminals, the first terminal of the second magnetic storage element being electrically connected to a second bit line and the second terminal of the second magnetic storage element being electrically connected to the first source/drain region of the second transistor; and

the second source/drain regions of the first and second transistors are electrically connected together.

16. The MRAM array of claim 14, wherein at least one of the first and second magnetic storage elements in the at least one memory cell comprises a magnetic tunnel junction (MTJ) device.

17. The MRAM array of claim 14, wherein the at least one memory cell further comprises a first conductive via electrically connecting the first magnetic storage element to the first transistor, and at least a second conductive via electrically connecting the second magnetic storage element to the second transistor.

18. The MRAM array of claim 14, wherein the at least one memory cell is configured such that a first write word line is formed on the first insulating layer and in close relative proximity to the first magnetic storage element, and at least a second write word line is formed

on the second insulating layer and in close relative proximity to the second magnetic storage element.

19. The MRAM array of claim 14, wherein the at least one memory cell is configured such that a bit line coupled to the memory cell is shared between the first and second magnetic storage elements associated with the memory cell.

20. The MRAM array of claim 14, wherein the at least one memory cell is configured such that a first write line coupled to the memory cell is shared between the first and second magnetic storage elements associated with the memory cell.

21. The MRAM array of claim 14, wherein the first and second magnetic storage elements associated with the at least one memory cell are substantially aligned along a vertical dimension relative to one another.

22. The MRAM array of claim 14, wherein the first and second magnetic storage elements associated with the at least one memory cell are substantially non-overlapping relative to one another.

23. A method of forming a memory cell, comprising the steps of:

forming at least first and second transistors in a semiconductor layer;

forming a first insulating layer on at least a portion of the first and second transistors;

forming a first magnetic storage element on at least a portion of the first insulating layer, the first magnetic storage element being electrically connected to the first transistor;

forming at least a second insulating layer on at least a portion of the first magnetic storage element; and

forming at least a second magnetic storage element on at least a portion of the second insulating layer, the second magnetic storage element being electrically connected to the second transistor.

24. The method of claim 23, further comprising the steps of:

forming a first conductive via in the semiconductor layer, the first conductive via electrically connecting the first magnetic storage element to the first transistor; and

forming at least a second conductive via in the semiconductor layer, the second conductive via electrically connecting the second magnetic storage element to the second transistor.

25. The method of claim 24, wherein forming each of the first and second conductive vias comprises the steps of:

forming an opening through at least one of the first and second insulating layers to expose at least a portion of the first source/drain region of a corresponding one of the first and second transistors; and

depositing an electrically conductive material in the opening so as to substantially fill the opening.

26. An integrated circuit device including at least one memory cell, the at least one memory cell comprising:

first and second transistors formed in a semiconductor layer;

a first insulating layer formed on at least a portion of the first and second transistors;

a first magnetic storage element formed on at least a portion of the first insulating layer, the first magnetic storage element being electrically connected to the first transistor;

at least a second insulating layer formed on at least a portion of the first magnetic storage element; and

at least a second magnetic storage element formed on at least a portion of the second insulating layer, the second magnetic storage element being electrically connected to the second transistor.